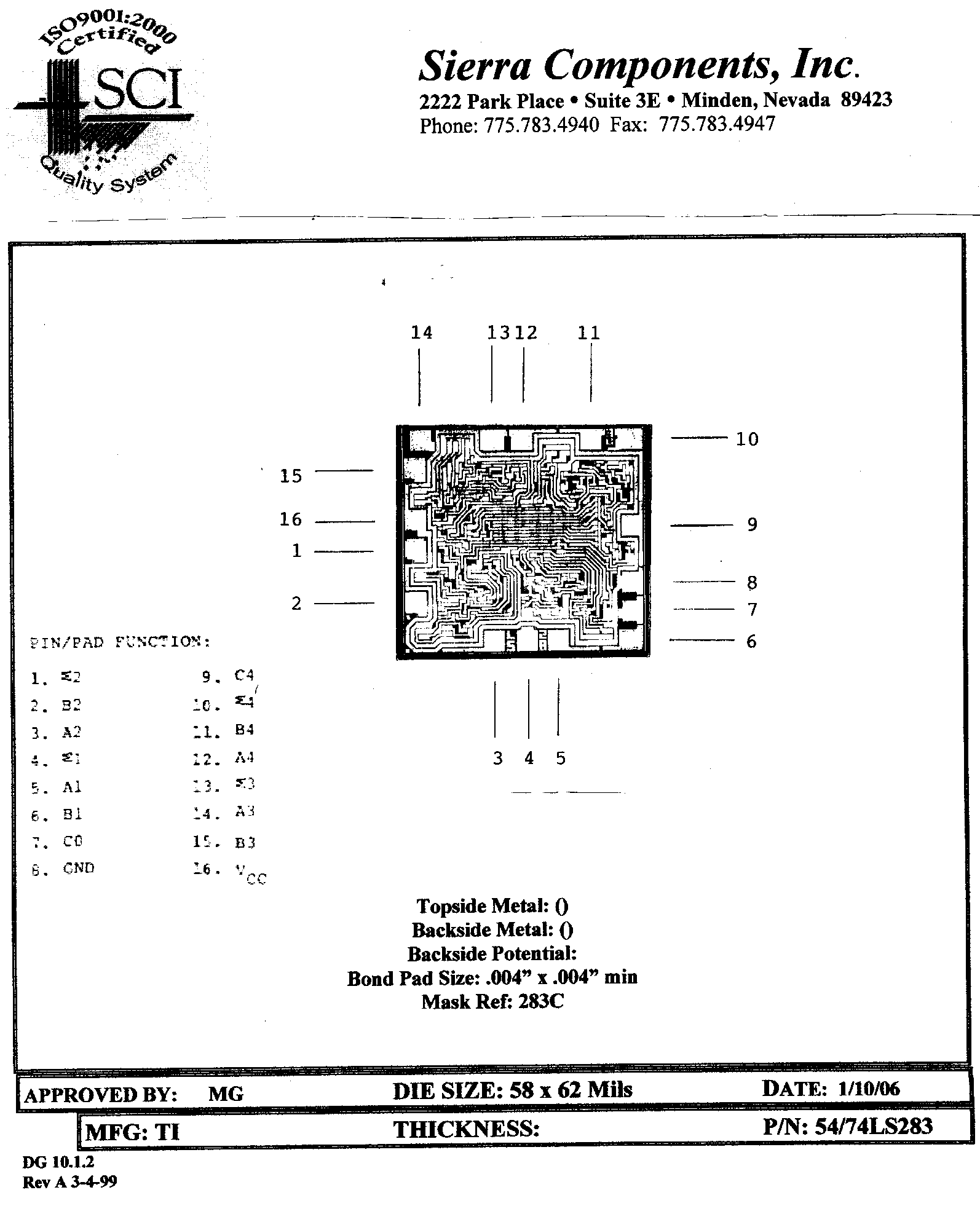
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

****

**.062”**



**.058”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004 x .004”**

**Backside Potential:**

**Mask Ref: 283C**

**APPROVED BY: DK DIE SIZE .058” X .062” DATE: 3/19/21**

**MFG: Texas Instrurments THICKNESS .000” P/N: 54LS283**

**DG 10.1.2**

#### Rev B, 7/1